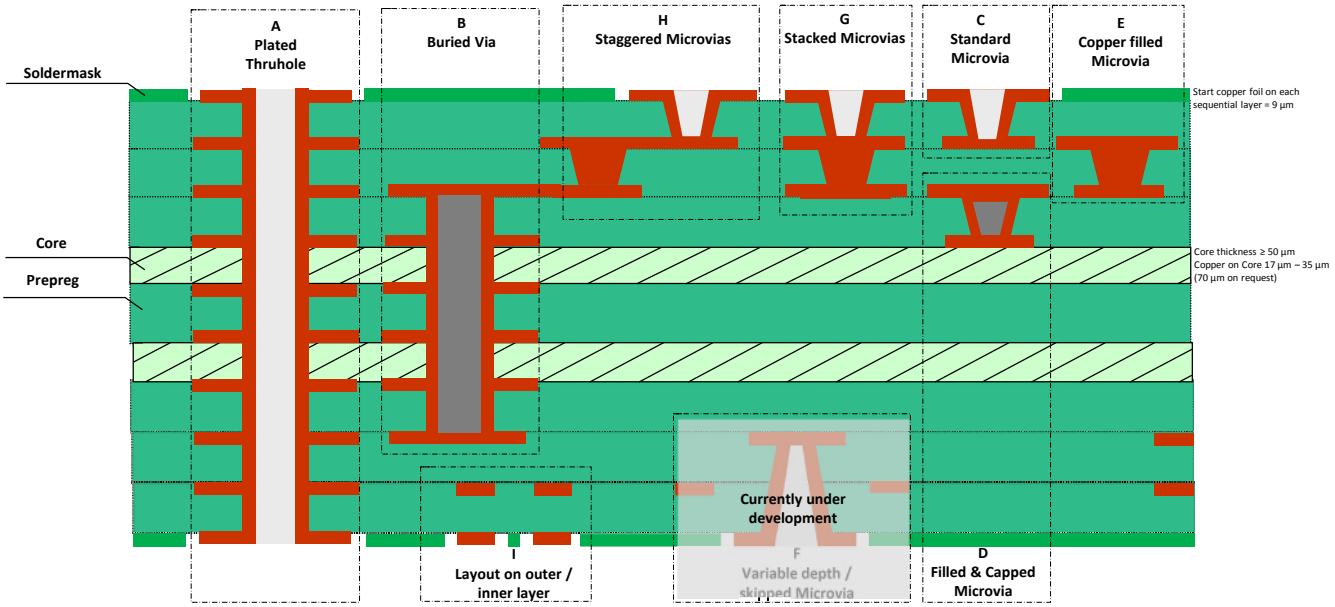
Design rules HDI-PCB

These rules apply in addition to the general design rules for multilayer PCB´s



A. Plated Thruhole see figure I. on page 2 **B. Buried Via**		**Value**
Minimum final diameter	Depending on Aspect Ratio	≥ 100 µm
Drilled diameter		= Final diameter + 100 µm
Maximum aspect ratio	Drilled diameter : Via depth	≤ 1:10
Minimum pad diameter outer layer up to 8 Layers		≥ Final diameter + 300 µm
Minimum pad diameter inner layer up to 8 Layers		≥ Final diameter + 350 µm
Minimum pad diameter outer layer > 8 Layers		≥ Final diameter + 300 µm
Minimum pad diameter inner layer > 8 Layers		≥ Final diameter + 400 µm

C. Standard Microvia see figure II. on page 2 **D. Filled & Capped Microvia** **E. Copper filled Microvia**		**Value**
Minimum diameter as formed	Depending on Aspect Ratio	≥ 100 µm
Maximum diameter as formed		≤ 150 µm
Final diameter		Diameter as formed – (plating x 2)
Minimum capture land	Acc. To IPC-2226 A, Level B	≥ Diameter as formed+ 175 µm
Minimum target land	Acc. To IPC-2226 A, Level B	≥ Diameter as formed+ 150 µm
Maximum aspect ratio	Diameter as formed : Via depth	≤ 1:1
Filling level copper filled via		75 % - 90 %

F. Variable depth / skipped Microvia see figure III. on page 2		**Value**
Currently under development		

G. Stacked Microvia see figure IV. on page 2		**Value**
Maximum cycles of stacked vias		4
All other values see: C. Standard microvias		

H. Staggered Microvia see figure V. on page 2		**Value**
Minimum staggered microvia pitch		≥ (Pad a + Pad b)/2

I. Layout on outer / inner layer see figure VI & VII. on page 2		**Value**
Minimum line / space		≥ 75 µm / ≥ 75 µm
Minimum distance wall to copper plated thruholes		≥ 250 µm
Minimum distance wall to copper microvia		≥ 162,5 µm
Minimum soldermask web	Green soldermask	≥ 80 µm
Minimum soldermask clearance		≥ 35 µm
Minimum soldermask overlapping (Soldermask defined pad)		≥ 35 µm

Your requirements violate our design rules? Please contact us. We will try to find an alternative solution with you.

Design rules HDI-PCB

Illustrated explanations of the terms

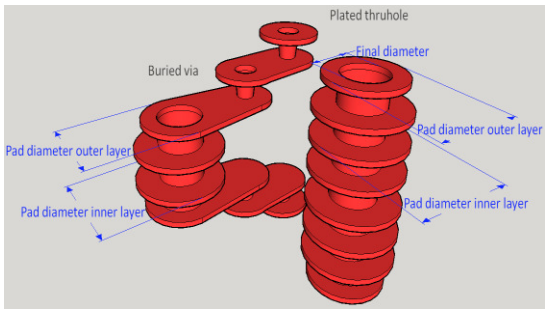


Figure I. Plated Thruhole & Buried Via

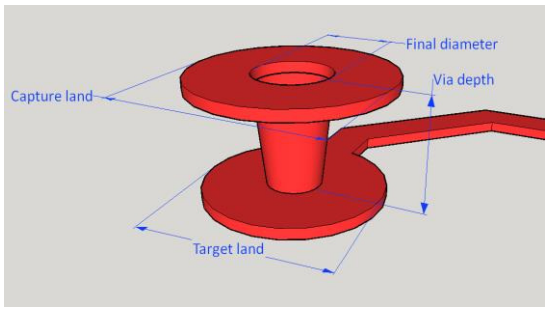


Figure II. Standard Microvia, Filled & Capped Microvia, Copperfilled Microvia

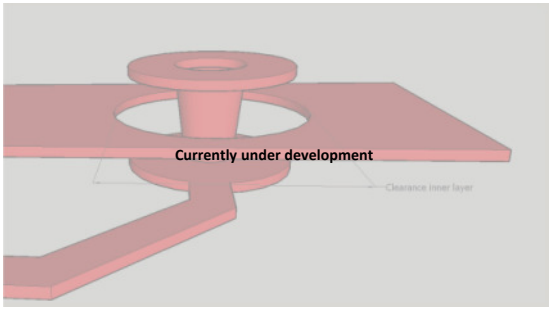


Figure III. Variable depth / Skipped Microvia

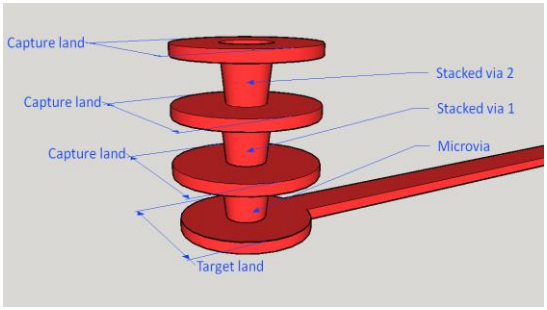


Figure IV. Stacked Microvia

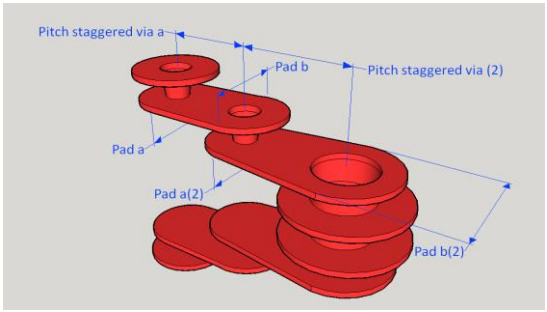


Figure V. Staggered Microvia

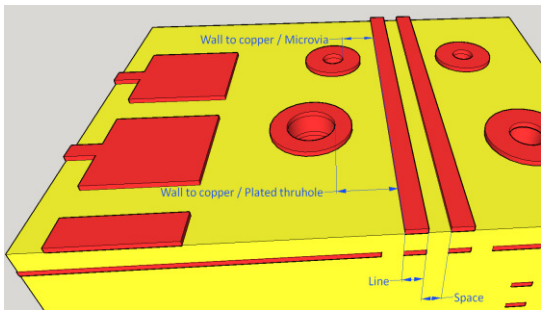


Figure VI. Copper layout on outer / inner layer

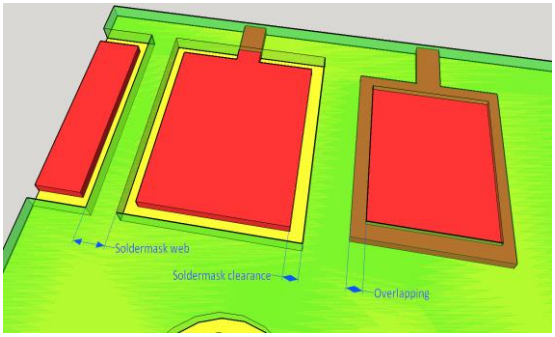
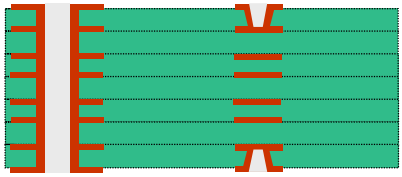


Figure VII. Soldermask layout on outer / inner layer

Design rules HDI-PCB

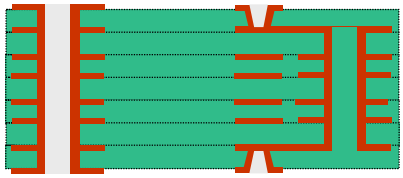
Decision Support HDI Strategy

The following six examples (based on the IPC 2226) are intended to facilitate a selection of the contacting strategy of HDI multilayers on the basis of their properties and complexity. The examples do not cover all possibilities, but provide a basic overview for determining the degree of complexity.



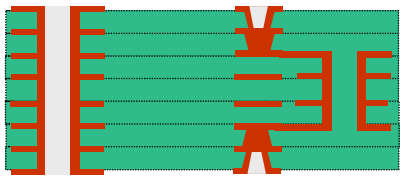
Type I acc. to IPC2226

This construction describes a multilayer in which there are both microvias and conductive vias used for interconnection. Type I constructions describe the fabrication of a single microvia layer on each side.
The PTH´s and the microvias can be optionally filled & capped (not shown).



Type II acc. to IPC2226

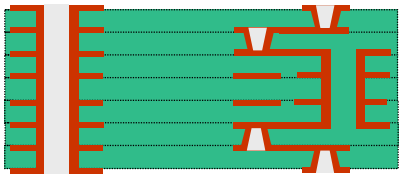
Type II constructions describe an HDI printed board in which there are plated microvias, plated buried vias, and may have PTHs used for top-to-bottom interconnection. The buried vias may be prefilled with a non-conductive paste or partially or completely filled with dielectric material from the lamination process.
The PTH´s and the microvias can be optionally filled & capped (not shown).



Type III acc. to IPC2226, example A (Stacked microvia)

Essentially corresponds to type II, but has at least two microvia layers on at least one side of a subcomposite core. The PTH´s and the microvias can be optionally filled & capped (not shown). As shown, internal stacked vias must be filled & capped or copper filled.

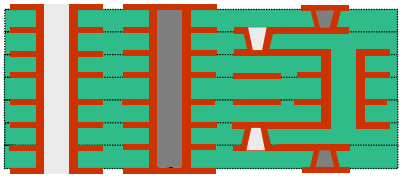
- Advantage: Stacked vias in combination with filling & capping or copper filling is a very space-saving method to enable a fanout also for multi-row finepitch-BGA´s.



Type III acc. to IPC2226, example B (Staggered microvia)

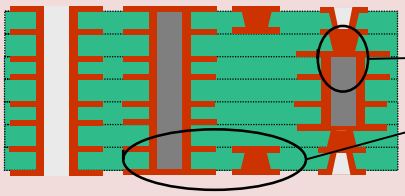
Essentially corresponds to type II, but has at least two microvia layers on at least one side of a subcomposite core. The PTH´s and the microvias can be optionally filled & capped (not shown).

- Advantage: The exclusive use of staggered microvias allows the use of conventional manufacturing technologies and offers a high degree of reliability and signal integrity. ILFA recommends this example.



Type III acc. to IPC2226, example C (Staggered microvia, filled & capped Via + microvia)

Essentially corresponds to type II, but has at least two microvia layers on at least one side of a subcomposite core.



Example D (Not recommended technologies)

- Stacking not recommended over resin or conductive/non-conductive filled vias due to potential for reduced
reliability. The use of staggered structures instead is recommended.

- The combination of copperfilled vias and filled & capped vias on same layers results in many process steps which negatively influence a defined copper layer thickness. Instead we only recommend filling & capping for both PTHs and microvias (shown in example C).

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Kalkmann, 07.02.2019